

A 200-Hz Bandwidth 120-dB SNDR Hybrid Delta Sigma modulator

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A delta-sigma ADC, operating for the 200 Hz signal bandwidth, is implemented in 180 nm CMOS, implementing oversampling as 1024, implementing 18bit resolution. The circuit is targeted for Bio-signal. The structure of Delta-sigma modulator is a third-order mixed op-amp loop filter using SC structure and RC structure. Double chopping, incremental structure is used to achieve resolution higher than 110dB. Therefore, we implemented the first integrator with discrete time, which is less affected by chopping switching and incremental switching. The second and third integrators are implemented in a continuous-time structure with good power efficiency compared to discrete-time. Because continuous-time delta-sigma modulator does not switch unlike discrete-time delta-sigma modulator. Therefore, low power design is easy. However, switching noise from the first integrator affects the 2,3 integrators and causes overall performance degradation. To address the performance degradation from switching noise, we designed a dead-time modulator between the first discrete-time integrator and the 2,3 continuous-time integrator. The Hybrid delta-sigma ADC achieves 115-dB SNR, 112.9-dB SNDR within a 200-Hz signal band while 1.2 mW from a 1.8 V supply.

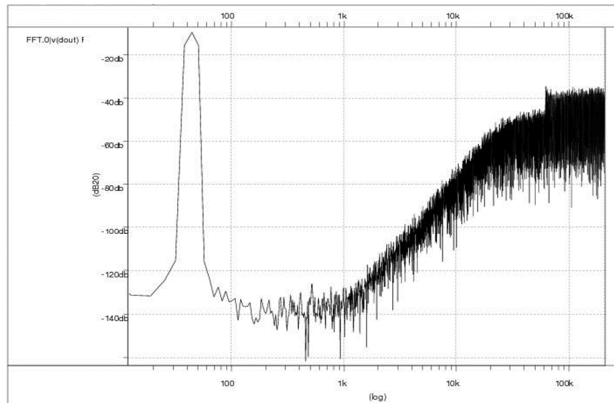


Fig1. Output spectrum of the delta sigma modulator

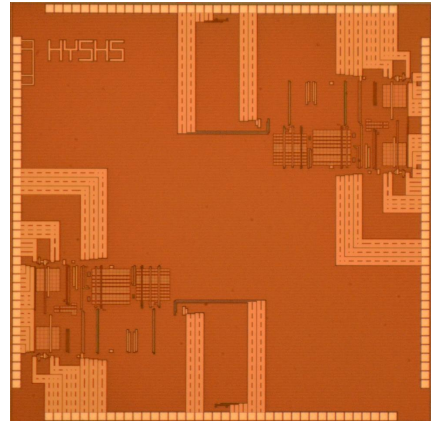


Fig2. Chip micrograph

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References [1] Y. Yoon, D. Choi, and J. Roh, "A 0.4-V 63-uW 76.1-dB SNDR 20-kHz Bandwidth Delta-Sigma Modulator Using a Hybrid Switching Integrator", *IEEE Journal of Solid-State Circuits*, vol. 50, no. 10, pp. 2342-2352, Oct. 2015. [2]] Q. Duan, Z. Wang, and J. Roh, "A 7.5-uW 0.08-mm² Single-Ended SC Delta-Sigma ADC for Acoustic Sensor Applications", *International Journal of Circuit Theory and Applications* . Sep. 2015.